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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/021,696	10/30/2001	Michael Eneboe	01-490	9160

24319 7590 06/11/2003

LSI LOGIC CORPORATION  
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MS D-106, LEGAL DEPARTMENT  
MILPITAS, CA 95035

EXAMINER

SIEK, VUTHE

ART UNIT	PAPER NUMBER
	2825

DATE MAILED: 06/11/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/021,696	ENEBOE ET AL.	
	Examiner Vuthe Siek	Art Unit 2825	
<b>-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --</b>			
<b>Period for Reply</b>			
<p>A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.</p> <ul style="list-style-type: none"> <li>- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.</li> <li>- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.</li> <li>- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.</li> <li>- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).</li> <li>- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).</li> </ul>			
<b>Status</b>			
<p>1)<input type="checkbox"/> Responsive to communication(s) filed on _____.</p> <p>2a)<input type="checkbox"/> This action is FINAL.                    2b)<input checked="" type="checkbox"/> This action is non-final.</p> <p>3)<input type="checkbox"/> Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i>, 1935 C.D. 11, 453 O.G. 213.</p>			
<b>Disposition of Claims</b>			
<p>4)<input checked="" type="checkbox"/> Claim(s) <u>1-23</u> is/are pending in the application.</p> <p>4a) Of the above claim(s) _____ is/are withdrawn from consideration.</p> <p>5)<input type="checkbox"/> Claim(s) _____ is/are allowed.</p> <p>6)<input checked="" type="checkbox"/> Claim(s) <u>1-13 and 16-23</u> is/are rejected.</p> <p>7)<input checked="" type="checkbox"/> Claim(s) <u>14 and 15</u> is/are objected to.</p> <p>8)<input type="checkbox"/> Claim(s) _____ are subject to restriction and/or election requirement.</p>			
<b>Application Papers</b>			
<p>9)<input type="checkbox"/> The specification is objected to by the Examiner.</p> <p>10)<input checked="" type="checkbox"/> The drawing(s) filed on <u>30 October 2001</u> is/are: a)<input checked="" type="checkbox"/> accepted or b)<input type="checkbox"/> objected to by the Examiner.</p> <p style="margin-left: 20px;">Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).</p>			
<p>11)<input type="checkbox"/> The proposed drawing correction filed on _____ is: a)<input type="checkbox"/> approved b)<input type="checkbox"/> disapproved by the Examiner.</p> <p style="margin-left: 20px;">If approved, corrected drawings are required in reply to this Office action.</p> <p>12)<input type="checkbox"/> The oath or declaration is objected to by the Examiner.</p>			
<b>Priority under 35 U.S.C. §§ 119 and 120</b>			
<p>13)<input type="checkbox"/> Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).</p> <p>a)<input type="checkbox"/> All b)<input type="checkbox"/> Some * c)<input type="checkbox"/> None of:</p> <p>1.<input type="checkbox"/> Certified copies of the priority documents have been received.</p> <p>2.<input type="checkbox"/> Certified copies of the priority documents have been received in Application No. _____.</p> <p>3.<input type="checkbox"/> Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).</p> <p>* See the attached detailed Office action for a list of the certified copies not received.</p>			
<p>14)<input type="checkbox"/> Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).</p> <p>a)<input type="checkbox"/> The translation of the foreign language provisional application has been received.</p> <p>15)<input type="checkbox"/> Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.</p>			
<b>Attachment(s)</b>			
<p>1)<input checked="" type="checkbox"/> Notice of References Cited (PTO-892)</p> <p>2)<input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)</p> <p>3)<input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) <u>2-3</u>.</p>		<p>4)<input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____</p> <p>5)<input type="checkbox"/> Notice of Informal Patent Application (PTO-152)</p> <p>6)<input type="checkbox"/> Other: _____</p>	

### **DETAILED ACTION**

1. This office action is in response to application 10/021,696 filed on 10/30/2001.

Claims 1-23 remain pending in the application.

#### ***Specification***

2. The disclosure is objected to because of the following informalities: information of co-pending applications is mission (see first paragraph on page 1).

Appropriate correction is required.

#### ***Claim Objections***

3. Claims 19-21 are objected to because of the following informalities: claim 19 should depend on claim 18; claim 20 should depend on claim 18; and claim 21 should depend on claim 18. The change would provide proper claim antecedent basis.

Appropriate correction is required. Examiner has examined these claims based on above suggestion.

#### ***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-13, 16-21 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsuzawa (6,505,329).

6. As to claims 1, 11 and 16, Matsuzawa teaches a method and system for designing an integrated circuit (IC) (see abstract; Figs. 3-10 and description) comprising receiving data specifying a plurality of interconnects and components of a design of an IC (interconnective information, design files Fig. 3); and optimizing the design of the IC, wherein data specifying the plurality of interconnects and devices (macros, circuit elements) of the IC is optimized based on at least one of bandwidth, latency, scalability, position of devices and interconnect configuration (col. 3, lines 52-67; col. 4, lines 1-31; col. 5, lines 42-67; col. 6, lines 1-63). In addition, Matsuzawa teaches that the IC design includes hard macros (firm macros) and soft macros as claimed. Therefore, an IC design should be produced as a self-programmable IC as claimed, wherein optimization is based in heuristic data (integrated hard macros and soft macros). It is noted that although, the term of optimization is not found in the cited portion, the objective of said designing an IC using the method and system as taught by Matsuzawa is toward design optimization, since it aims toward reducing size of a target IC design.

7. As to claims 2-4, Matsuzawa teaches a system and method that can be used to integrate macros and soft macros (cores) into a single chip design in order to obtain highly integration chip to improve the design efficiency, to design a downsized semiconductor device, to hold down the performance deterioration, to prevent circuit performance from differencing in each semiconductor device made into new products and to prevent the performance of devices from differing in each product or each semiconductor device. Therefore, the designed product or new product produced by the method and system as taught by Matsuzawa would be obtained by programming

Art Unit: 2825

the optimized data (integrated design files of hard macros, soft macros and their interconnective information) into a self-programmable IC. In addition, the optimized design (integrated design files of hard macros, soft macros and their interconnective information) includes a specified characteristic for the interconnect, wherein the specified characteristic inherently includes at least one of bandwidth, latency and scalability (col. 6).

8. As to claims 5-10, 12-13, 17-21 and 23, Matsuzawa teach interconnective information is used to synthesize or produce an IC design, arranging components of the IC (included within the operation of layout design; col. 6); wherein the specifying bandwidth is inherently within the IC design (as Matsuzawa teach IC design application include in the field of mobile communication device, package downsizing, energy efficiency of highly demand of core semiconductor devices such as single-chip microcomputers, col. 3, lines 40-50); wherein the components (hard macros, soft macros, circuit elements, or cores, some are considered as predefined devices) are arranged (performed by a layout design unit in Fig. 3) based on latency (inherently within IC design), scalability, timing considerations, power considerations, data switching and bandwidth or amount of data transferred (col. 3, lines 40-67; col. 4, lines 1-31). Matsuzawa teach an IC design to produce single-chip microcomputers including integration of hard macros, soft macros and interconnective information by a data processing system operable by a computer program application (Figs. 3, 4, 7, 8, 10). The optimization by the system and method is done by layout design unit, meaning the it is done without user intervention by an agent. Matsuzawa teach IC design application

Art Unit: 2825

including ASICs (col. 1). The interconnects not specified by a user are automatically configured by an agent (layout design unit, Fig. 3). In addition, Matsuzawa teach producing single chip microcomputers and multiple integrated circuit solution (col. 3, lines 40-50).

***Claim Rejections - 35 USC § 103***

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claim 22 rejected under 35 U.S.C. 103(a) as being obvious over Matsuzawa in view of Boyle et al. (6,557,145).

11. As to claim 22, Matsuzawa does not teach optimization includes partitioning, although is known to one of ordinary in the art. Boyle et al. teach concurrent design optimization comprising partitioning based on cost considerations (Figs. 7A-7B).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include optimization with partitioning based cost functions in Matsuzawa IC design system in order to further improve chip design to obtain desired downsized semiconductor microcomputers.

***Allowable Subject Matter***

12. Claims 14-15 are objected to as being dependent upon a rejected base claim(s), but would be allowable if rewritten in independent form including all of the limitations of

Art Unit: 2825

the base claim and any intervening claims, since the prior art does not teach of fairly suggest the amount of data transferred over the first interconnection is less than an initially determined bandwidth, bandwidth of the first interconnection is decreased; and the amount of data transferred over the first interconnection is greater than an initially determined bandwidth, bandwidth of the first interconnection is increased.

### ***Conclusion***

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (703) 305-4958. The examiner can normally be reached on M-F (6:30-4:00) 2nd Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703) 308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Vuthe Siek  
Primary Examiner  
June 4, 2003

*Vuthe Siek*  
VUTHE SIEK  
PRIMARY EXAMINER